

REMARKS/ARGUMENTS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects claims 1-4, 8, 12, 16-25 under 35 U.S.C. 102(b) as being anticipated by Wei et al. The Examiner states that Wei discloses an image sensor with a plurality of rows of pixels and associated circuits and a plurality of columns and associated circuits. The Examiner states that it is disclosed in column 9 that the display is sequentially reset row-by-row, and column by column without resetting the entire display. The Examiner also states that Wei discloses in column 4, lines 3-33 that they are separately addressable line segments within the individual rows of the CCD.

We cannot agree. First of all, the Examiner's interpretation of Wei means that each of the pixel elements is a separate segment and therefore Wei does not show the limitation of the present claims which states there are a plurality of pixel circuits within each segment. Furthermore, the individual pixel circuits of Wei do not have electrically separate segments, that is, in order to avoid short circuiting the row and column lines and in order to reduce the capacitance on the lines, the row "segments" are electrically connected through each pixel element, see column 4, lines 8-18. In sharp contrast, each segment containing a plurality of pixel circuits of the present invention are electrically separate and therefore separately addressable. Furthermore, the control circuits of the present invention are separate for each of the segments of pixel circuits, in contrast to Wei et al. In addition, the control signals of the present invention are D.C. coupled to the segments of pixel circuits, whereas all the control signals in Wei et al are capacitively coupled and therefore use A.C. coupled signals. Claims 1 and 19 have been amended in order to clarify these distinctions.

The Examiner rejects claims 5-7 and 13-15 under 35 U.S.C. 103(a) as being unpatentable over Wei et al. The Examiner states that Wei does not specifically disclose logic gates but does disclose that transfer gates are used. The Examiner states that logic gates are old and well known and concludes that it would have obvious to a person of ordinary skill in the art at the time the invention was made to use logic gates as the

gates of Wei in order to allow for binary manipulation of the signals and for saturation considerations.

We cannot agree. It should be noted that the transfer gates referred at column 2, line 12 are for the readout of the data, not the generation of the control signals. Furthermore, as is well to those skilled in the art, transfer gates can pass A.C. signals whereas logic gates are D.C. coupled. In addition, these claims are dependent directly or indirectly from claim 1, and are therefore patentable for the same reasons.

Accordingly, applicants believe the application as amended, is in condition for allowance for allowance, and such action is respectfully requested.

Respectfully submitted,

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